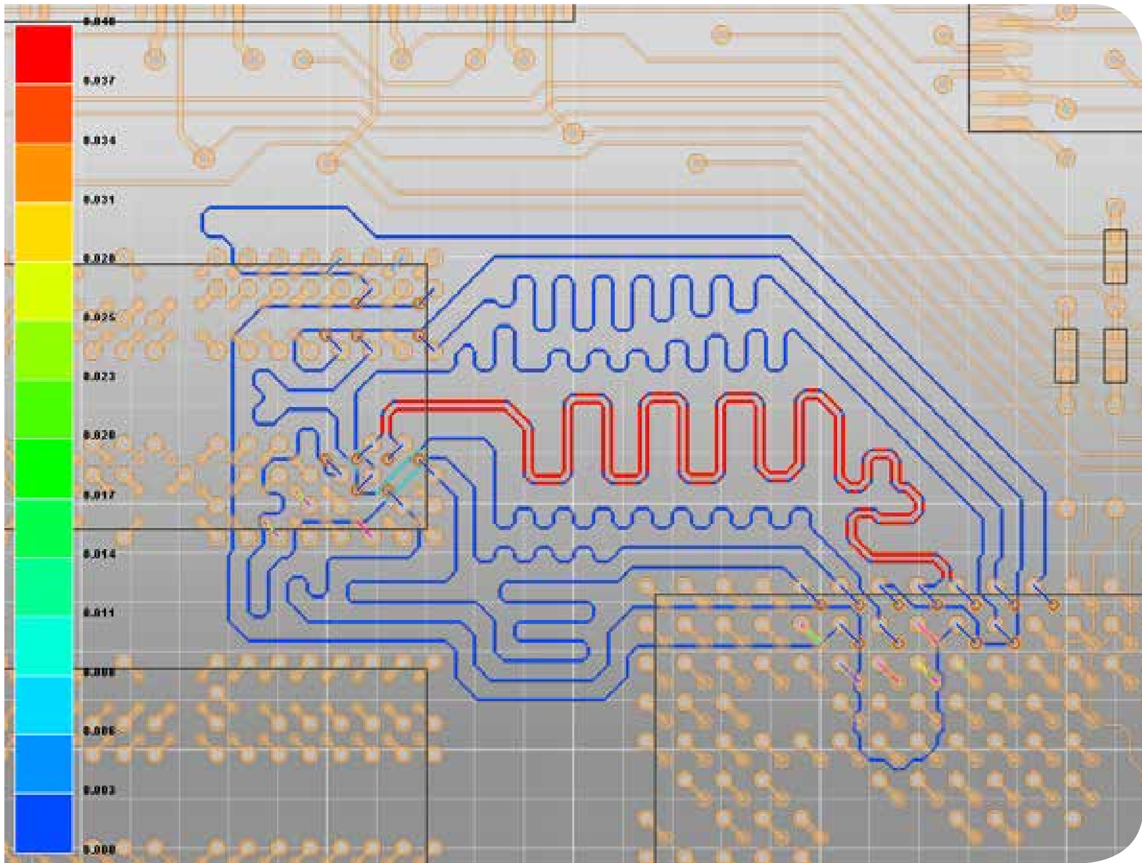
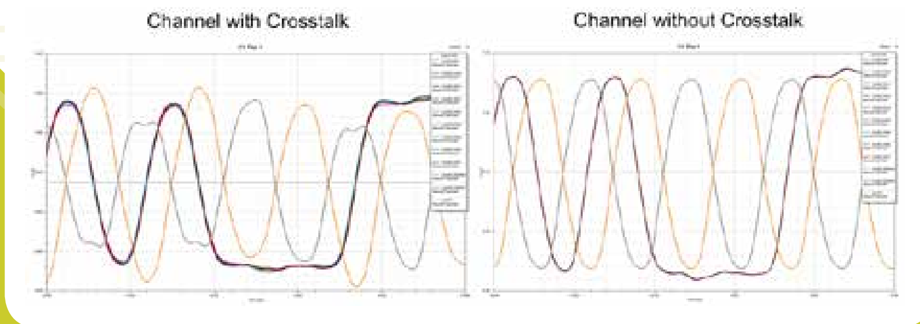


A VIA RUNS THROUGH IT

Signal integrity has emerged as a major issue in the design of high-speed electronics. While signal crosstalk has been a challenge for electrical engineers for some time, the proliferation of electronics in our lives amplifies the negative consequences of bad design practices. The ANSYS Electronics Desktop, which includes enhancements to ANSYS HFSS and ANSYS SIwave, is an essential tool for engineers looking to address electronic system reliability issues, such as signal integrity, power integrity and EMI/EMC. Interconnect Engineering, Inc. used these simulation tools to analyze a customer case involving a DDR3-800 board. They determined that unexpected crosstalk was originating in the BGA vias, and solved the problem by routing layers closer to the primary side of the PCB.

By **Stephen P. Zinck**, President, Interconnect Engineering, Inc., North Berwick, USA



Waveform results from ANSYS SIwave simulation unexpectedly showed that DQS signals had serious signal integrity issues due to suspected crosstalk.

Before there was mainstream signal integrity (SI) analysis, there was crosstalk. Typical of early designs was a Micro Channel, 10 Mbit/s Ethernet card for the IBM PS/2. The proof of concept prototype was actually a programmable array logic (PAL)-based design that was physically wire-wrapped on an off-the-shelf development board. This board had thousands of little green, blue, yellow and red wire connections and wire-wrap pins that were crowded together, creating a potential crosstalk nightmare. But this design worked because the timing margins were fairly large and the edge-rates were extremely slow. Electronics design and verification engineers abandoned this laborious build-and-test workflow as soon as it was practical to do so.

Today's High-Speed Crosstalk Challenges

Wire-wrap board designs were soon obsolete when crosstalk became a very real concern with the advent of high-speed electronics. The traditional forms of crosstalk still pose problems for today's high-density designs. The use of dual stripline printed circuit boards (PCBs) can cause crosstalk problems, especially since the breakout trace lengths from ball grid arrays (BGAs) can be long enough to cause crosstalk saturation with today's fast edge-rate silicon. Every designer knows the most obvious crosstalk cases to avoid, such as line-to-line spacing on the same layer. Crosstalk occurs in connector systems and device packages, but is also lurking in areas that might surprise some designers.

Customer Analysis Case: DDR3-800

Interconnect Engineering, Inc. was given the task of analyzing a customer's DDR3-800 board, which poses no challenges from a speed or technology perspective. The initial SIwave extraction produced valid, causal and passive S-parameter results that were imported and simulated in the Designer SI DDR3 environment that had been previously constructed. But these simulations also produced results that were unexpected. The waveform results showed that the DQS signals (qualifying signals indicating whether the data is valid) had serious signal integrity issues due to suspected crosstalk. This crosstalk also shifted the edges of the DQS signals such that flight-time variation relative to the rest of the byte-lane group was occurring. When the channel was simulated without exciting the neighboring members of the byte-lane group, the signal integrity and flight-time skew were normalized. Deeper inspection would be required to understand these deleterious effects.

Finding the Source of Crosstalk

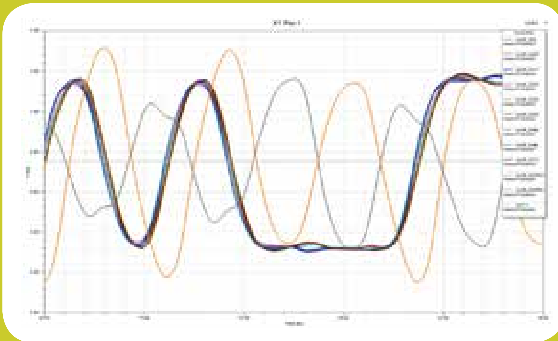
ANSYS SIwave contains a new, powerful engine to find sources of crosstalk. With very little setup time required, SIwave presents a whole host of analyses and results to parse. Interconnect Engineering, Inc. used SIwave and discovered that, for this design, the near-end crosstalk result showed anomalous behavior.

The DQS signals highlighted in red had crosstalk effects, but, strangely enough, they did not occur at the destination, which would have pointed to line-to-line spacing violations. The company that had done the layout of the DDR3 interface had taken great precautions to make sure the edge-to-edge crosstalk spacing constraints were much greater than one would have expected, so this was not the cause of the crosstalk.

Engineers then turned to ANSYS HFSS, with its 3-D field-solving capabilities, to solve the crosstalk mystery. The database was imported into HFSS, and,

again, causal and passive S-parameters were extracted and imported into the Designer SI circuit simulator for validation. The results showed that the same phenomenon was present using either tool (SIwave or HFSS).

ANSYS Electronics Desktop determined that the customer had routed and constrained their own design with very good crosstalk rules, but simulation showed that, in fact, there was significant crosstalk occurring between signals. The signals in question were not even routed next to each other on the same layer. The source of the crosstalk was not coming from the routing per se; it was coming from adjacent vias in the BGA footprint area. These BGA pins could not be changed as the device was a commercially produced processor.



Designer SI circuit simulator results showed that the same crosstalk phenomenon was present using either ANSYS SIwave or ANSYS HFSS.

So it appeared that this crosstalk was embedded into the design without the designer's knowledge or their ability to change anything to ward off its effects.

Reducing Crosstalk

The PCB stackup the customer used was quite thick with many layers. The layers they used to route the interface happened to be close to the secondary side of the stackup. Interconnect Engineering, Inc. postulated that if BGA footprint via crosstalk was an issue, reducing via parallelism would help the situation. ANSYS Electronics Desktop was again used to change the layers of the routing to more favorable layers that were closer to the primary side of the board to see if this would solve the problem.

One More Tool for the Toolbox

The results are clear: Using layers closer to the primary side will yield less crosstalk for any system, especially for high-speed systems (DDR4, 28Gb/s, 100Gb/s, etc.). Engineers can no longer think about — or simulate — designs in two dimensions; they must adopt a 3-D perspective. BGA footprint vias are not as benign as we would like to think. So one more rule can be added to the designer's toolbox: Utilize routing layers closer to the primary when trying to reduce crosstalk for critical interfaces. The source of the crosstalk was not obvious, but could only be discovered using state-of-the-art simulation tools from ANSYS.

Reduced crosstalk resulting from using layers closer to the primary side

Using the full functionality of the ANSYS Electronics Desktop enabled Interconnect Engineering, Inc. to analyze, diagnose and implement a solution for the customer's crosstalk issue, which would have resulted in at least one costly re-spin to solve the problem. Without ANSYS solutions, they may have never found the true culprit causing the crosstalk. The engineers may have had to resort to slowing down the memory interface in order to be able to ship product with sub-par bandwidth performance. Project schedule, cost and performance all would have suffered. ANSYS Electronics Desktop enabled Interconnect Engineering to ship the best-performing product on time and on budget. Λ

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